



The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology

By Ray Salemi



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The UVM Primer uses simple, runnable code examples, accessible analogies, and an easy-to-read style to introduce you to the foundation of the Universal Verification Methodology. You will learn the basics of object-oriented programming with SystemVerilog and build upon that foundation to learn how to design testbenches using the UVM. Use the UVM Primer to brush up on your UVM knowledge before a job interview to be able to confidently answer questions such as "What is a uvm_agent?", "How do you use uvm_sequences?", and "When do you use the UVM's factory." The UVM Primer's downloadable code examples give you hands-on experience with real UVM code. Ray Salemi uses online videos (on uvmprimer.com) to walk through the code from each chapter and build your confidence. Read The UVM Primer today and start down the path to the UVM.

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Editorial Review

About the Author

Ray Salemi is a senior verification consultant with Mentor Graphics. Salemi started his career in Electronic Design Automation with Gateway Design Automation, the inventors of Verilog. Since then he has worked for Cadence Design Systems, Sun Microsystems, and several startups. Ray Salemi is the author of the popular introduction to simulation, FPGA SIMULATION.

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