



Nanometer Variation-Tolerant SRAM: Circuits and Statistical Design for Yield

By Mohamed Abu Rahma, Mohab Anis



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Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power.

This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies.

- Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques;
- Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view;
- Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.

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Editorial Review

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